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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 16

Application Number: 09/410,202

Filing Date: 9/30/1999

Appellant(s): Donovan

William O. Geny

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 17, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The two amendments after final have been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellent provides separate arguments for independent claims 4 and 10. The claims are grouped as follow:

Group I, claims 2, 4-7 and 14-16. Appellent provides arguments on claim 4 but no arguments as to why claims 2, 5-7 and 14-16 are patentable over Madnick (the applied reference, a text book). Claims 2, 5-7 and 14-16 stand or fall with claim 4.

Group II, claim 8. Appellant provides no separate arguments as to why claim 8 is patentable over Madnick in view of George. Claim 8 is dependent upon independent claim 4. Claim 8 therefore stands or falls with claim 4.

Group III, claims 9 and 10-13. Appellant provides separate arguments on claim 10 but no separate arguments as to why claims 9 and 11-13 are patentable over Madnick in view of Jen. Claims 9 and 11-13 stand or fall with claim 10.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct except for claims 4 and 9.

Claims 4 and 9 appeared on page 2 of Appendix are incomplete. A complete copy of claim 9 appears on page 3 of the Appendix. A complete claim 4 is reproduced as follow:

4. In a microprocessor-based computing system having a CPU for executing tasks represented by task register sets and further including peripheral devices that issue interrupt commands, an interrupt and task change processing circuit comprising:

(a) a task enable circuit for determining from predetermined inputs whether a predetermined task is ready for execution by the central processing unit,

(b) a task priority selection circuit coupled to an output of the task enable circuit for determining an order for the running of tasks that have been determined ready for execution by the task enable circuit; and

(c) a task switching circuit coupled to an output of the task priority selection circuit for controlling the execution of tasks in a sequence determined by the task priority selection circuit.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,888,691	George et al.	12-1999
3,789,365	Jen et al.	1-1974

Madnick, S.E. "Operating System", Text book, McGraw-Hill, 1974. Pages 209-240.

Page 572 of Madnick is provided for the showing (in the Examiner's rebutal to the Appellant's arguments) that the advent of microprocessor is prior to the filing date in response to Appellant's new arguments presented in the brief. Page 572 is not applied in any of the rejections.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

(A) 35 U.S.C. 112, second paragraph rejection.

Claim 8 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 fails to recite functinal relationship between the trace enable circuit and any circuit components recited in parent claim 4 (MPEP 2172.01). The trace enable circuit is recited in dependent claim 8 for the purpose of recording register states of selected registers. There are no selected registers recited in the interrupt and task change processing circuit of parent claim 4. It is not clear how the trace enable circuit provides any useful function in interrupt and task change processing. The trace enable circuit as recited in claim 8 is a stand alone circuit which has nothing to do with interrupt and task change processing. The boundaries of what constitutes infringement of the patent therefore can not be determined (MPEP 2173).

(B) Art Rejection, Group I.

Claims 2, 4-7 and 14-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Madnick (text book).

Madnick taught:

Claim 4. In a microprocessor-based computing system (well known) having a CPU (inherent in a microprocessor) for executing tasks (see "--tasks he wants the computer system to perform for him" in the 4th paragraph of page 209 of Madnick) represented by task register sets (the status registers representing tasks inherent in Submit, Hold, Ready, Waiting, Running and Complete stages. See Figure 4-1 on page 210 of Madnick) and furthing including peripheral devices (mouse, keyboard, printer, etc., well known prior to filing date.) that issues interrupts commands (mouse signals, key codes generated by the keyboard, printer signals asking for CPU time), an interrupt and task change processing circuit (JOB SCHEDULER and PROCESS SCHEDULER in Figure 4-1, page 210 of Madnick) comprising:

(a) a task enable circuit for determining from predetermined inputs whether a predetermined task is ready for execution by the central processing unit (JOB SCHEDULER of Madnick in Figure 4-1 for placing tasks in Ready stage if they are ready for execution. See also page 212.),

(b) a task priority selection circuit coupled to an output of the task enable circuit for determining an order for the running of tasks that have been determined ready for execution by the task enable circuit (see item 2 in Section 4-1.1 of page 212 in Madnick. See also the third paragraph in Section 4-2 of page 215), and

(c) a task switching circuit coupled to an output of the task priority selection circuit for controlling the execution of tasks in a sequence determined by the task priority

selection circuit (PROCESS SCHEDULER in Figure 4-1 of page 210. See also Section 4-1.2 on pages 212 and 213.).

Figure 4-1 of Madnick does not show any rectangular boxes representing circuits. It is noted that claim 4 is not a circuit claim because claim 4 does not recite any electronic circuits (such as counters, multiplexers or registers etc.) depicted in Appellant's drawings. Although claim 4 uses the term circuit, it is actually a means plus function claim. The functions of JOB SCHEDULER and PROCESS SCHEDULER shown in figure 4-1 of Madnick are meant to be carried out by a computer. The only human portion is at the Submit Stage. One of ordinary skill in the art would readily realize that the portions of the computer which carry out the functions recited in the claims are circuits.

Claim 2. A method for ordering the performance of tasks in a computer system (execute the Schedulers of Madnick shown on Figure 4-1 by a microprocessor-based processor), said computer system having input sources (JOB SCHEDULER requesting tasks to be put from ready stage to run stage) that issue interrupt signals for requesting the performance of a task, said method comprising:

(a) providing an integrated circuit having circuit components for automating the selection of tasks to be performed by said computer system (execute the schedulers on a microrpocessor-based computer);

(b) wherein the integrated circuit performs the following steps:

(i) assigning a priority level for each task based upon a selected parameter of an interrupt signal (see item 2 in Section 4-1.1 of page 212 in Madnick. See also the third paragraph in Section 4-2 of page 215)

(ii) changing each priority level as a function of time (see page 215, section 4-2, third paragraph: "It takes into account not only the time a job arrives--"); and

(ii) beginning the execution of a first task when said priority level of said first task exceeds said priority level of all othe tasks.

Madnick does not show an integrated circuit. Microprocessor fabricated on an IC chip is well known in the art. One of ordinary skill in the art should readily realize that the sechedulers of Madnick can be executed by a microprocessor.

With respect to claims 5, and 14-16, attention of the Board is respectfully directed to page 215, section 4-2, third paragraph: "It takes into account not only the time a job arrives--". Madnick taught that job scheduling is a function of time.

With respect to claim 6, the Traffic controller (page 212) keep track of all the processes of a job and of different jobs.

With respect to claim 7, see "round robin" under the title "Typical process scheduling policies" on page 237.

No separate arguments are provided by Appellant in his brief for claims 2, 5-7 and 14-16. Claims 2, 5-7 and 14-16 therefore stand or fall with claim 4.

(C) Art Rejection, Group II.

Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Madnick in view of George (USP 4,888,691).

Madnick taught claim combination set forth above. Further, Madnick, in the first paragraph of page 209 and page 212, taught a traffic controller for keeping track of status of all processes. Madnick does not have a trace for recording state information. However, George taught a trace circuit for recording state information when interrupts happened. Attention of the Board is respectfully directed to column 3 et seq line 19 and column 21 et seq lines 25. Since both references are directed toward interrupt, it would have been obvious to a person of ordinary skill in the art to incorporate a trace circuit as taught by George in the traffic controller of Madnick such that state information can be retrieved when needed.

No separate arguments are provided by Appellant in his brief for claim 8. Claim 8 which is dependent on claim 4 therefore stands or falls with claim 4.

(D) Art Rejection, Group III.

The rejction of claims 9 and 10-13 based on 35 USC 103(a) over Madnick in view of Jen is hereby withdrawn in view of Appellant's arguments in his brief.

Claims 9 and 10-13 are allowed.

(11) Response to Argument

On page 4, Appellant states "the book(Madnick, applied text book) was written in 1974, well before the advent of the microprocessor). The statement is incorrect. The description on page 572, under section 10-2, the third line of entry "Ahearn, G. R. -- Jan. 1972" : "This article illustrates the use of microprocesors to produce sophisticated--control units" evidences that

microprocessor was well known prior January 1972. The schedulers of Madnick could have been executed on a microprocessor-based computer system.

At the top of page 5, Appellant states that rules in Madnick are applied by human decision. The statement is incorrect. The only human portion shown in Figure 4-1 of Madnick is at the Submit Stage. All other rules or decisions in Madnick are implemented by machine and not human being. In fact, the entire chapter 4 of Madnick is devoted to how jobs once submitted are scheduled by a computer to be executed such that processor time is used most efficiently.

In the second half of page 5, Appellant argues limitations which are not in the claims. There are no internal logics or electronic circuits recited in the claims. Although the apparatus claims use the term circuit, the apparatus claims do not recite any electronic components such as counters, registers or multiplexers pepicted in the drawings as argued by Appellant. In fact, the apparatus claims are actually means puls function claims. Appellant does not disagree that the functions of the schedulers of Madnick are carried out by computer circuits. The circuits in the computer which runs the schedulers of Madnick correspond to the circuit components of the claims as demonstrated in the rejections above. With respect to "providing an integrated circuit" of claim 2, Appellant does not claim that the invention is IC chip. The specificatin does not disclose how an IC chip is made. IC chip and fabricating of microprocessor on an IC are well known prior to the filing date of the instant application. Microprocessor is well known prior to 1972. The limitation of providing an IC is met by executing the schedulers of Madnick by a microprocessor on a chip.

With respect to the "real time" issue at the top of page 6, the argument is not understood. No real time is recited in the claims. Since Madnick meets all the claim limitations as demonstrated in the rejections, Madnick is just as real time as the system recited in the claims.

With respect to the limitation of peripheral devices, peripheral devices are inherent in a computer system as demonstrated in the rejections above.

With respec to Appellant's arguments directed to George (USP 4,888,691) on page 6, the George reference is applied for the trace limitation of claim 8 and not for the circuit limitation in claim 4.

With respect to the arguments directed to the Jen reference (USP 3,789,365) on pages 6 and 7, Jen is cited for the rejction of claims 9 and 10-13 and not for the rejction of claim 4 as argued by Appellant. Since the rejection of claim2 9 and 10-13 is withdrawn, the arguments are considered moot.

At the bottom of page 6, Appellant contends that there is no suggestions in either Madnick or George that suggests the combination that the Examiner wishes to make. The argument is direct to the rejection of claim 8 only because the rejection of claims 2, 4-7 and 14-16 is based on Madnick alone. The George reference is cited for the teaching of trace circuit recited in claim 8. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the rejection, the Examiner

suggests that Madnick taught a task processing circuit as claimed in pareent claim 4 and George taught a trace circuit for recording state information when interrupt happened in column 3 line 19 and column 21 line 25, and since both references are directed toward interrupt, it would have been obvious to a person of ordinary skill in the art to incorporated a trace circuit as taught by George in Madnick such that state information can be retrieved later for analysis. Further, in lines 7 and 8, of page 209, Madnick suggests that the status of processes should be traced. Appellants fails to provide any persuasive arguments as to why Madnick and George can not be combined as suggested by the Examiner. Appellant merely uses their own interpretation of the applied references and then conclude that they can not be combined based on their interpretation of the references. Further, as pointed out in the section 112, rejection of cliam 8, there is no functional relationship (combinability) between the trace circuit (taught by George) recited in claim 8 and the processing circuit recited in parent claim 4 (taught by Madnick). The trace circuit as recited in claim 8 is a stand alone circuit and can not be combined with the task processing circuit of parent claim 4.

With respect to the arguments directed to claim 4 on page 7, Appellant simply points out what a claim requires with no attempt to point out how the claim patentably distinguish over the prior art. This does not amount to a separate argument for patentability. In re Nielson, 816 F.2d 1567, 2 USPQ 1525 (Fed. Cir. 1987). Further, as demonstrated in the rejection above, Madnick meets all the claim limitations of claim 4.

With respect to the arguments directed to claim 10 on page 7, the rejection is withdrawn and therefore is considered moot.

With respect to the argument on page 8, the Magar and the Rubin references are cited (not applied in any of the rejections) in the Final Rejection. The Magar and the Rubin references were referenced in the Examiner's remark section of the Final Rejection for showing that integrated circuit chip (IC) and microprocessor are well known in the art prior to the filing date. Since Magar and Rubin are not applied in any of the rejections and are not referenced by the Examiner in his Answer, Appellant's remarks directed to the Magar and the Rubin references are considered moot.

In conclusion, Appleant's claimed invention is not an IC chip. Appellant's claimed invention is task scheduling carried out by a microprocessor-based computing system. Madnick taught a scheduler which performs all the functions recited in the claims. The scheduler of Madnick is executed on a microprocessor-based computer system. Circuits in the microprocessor perform all the functions of the scheduler. Microprocessor and IC are well known prior to the filinf date. The rejections are believed to be intact. Accordingly, it is respectfully requested that the Final Rejections of claims 2, 4-8, and 14-16 be sustained.

Respectfully submitted.

DAVID Y. ENG
PRIMARY EXAMINER

conferee: Eric Coleman E.C.

Daniel Pan D.P.